MMIC SSB Frequency Translators with Image-Rejection for Satellite Transponder Applications

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Abstract

A highly integrated design for advanced monolithic single side-band frequency translators are presented in this paper. Two monolithic chips have been realised which exhibit between 18-45dB of upper side-band rejection over C, X, and Ku-band. The chips are designed for small band-to-band frequency translations (such as uplink to downlink) in satellite communications transponders. Since the chips exhibit a wide-band response, image-rejection is also obtained for both chips.

Introduction

Frequency translators are a key component in virtually all microwave systems. When a mixer is used to perform a small frequency translation on an RF signal, output signals having spectral components at the sum and difference frequencies of the two inputs are generated (along with other signals). The sum frequency components are designated the upper side-band (USB) components while the difference frequency components are designated the lower side-band (LSB) components. A single side-band (SSB) frequency translator is thus of particular importance since it removes the unwanted side-band, and so prevents it from interfering with other transmissions.

A suitable topology for a small-shift SSB frequency translator is shown in fig.1. This requires two balanced mixers, 90^{o} RF hybrid, 0^{o} IF hybrid and a 90^{o} LO phase splitter. The key to an effective design is to have well matched amplitude and phase characteristics in the balanced mixers and hybrids. If the complete circuit is to be included on one singe substrate, maintaining the amplitude and phase balance becomes much more difficult in a hybrid design than a monolithic design because reproducibility is much more difficult in hybrid designs. Furthermore, for commercial satellite applications it is very desirable (and perhaps even necessary) to realise the circuits in monolithic form.

Two highly integrated monolithic SSB frequency translators have been realised for applications in satellite communications transponders in which the RX signal is directly translated to the TX frequency (which is higher than the LO frequency). A minimum of 18dB upper side-band (USB) rejection over the RF range 4.25-13.75GHz is obtained from the first chip, while a minimum of 23dB USB rejection over 16-19.75GHz RF is obtained for the second chip. Both chips, by virtue of their wide-band performance, also exhibit image-rejection.

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Circuit Topology

Fig.1 shows the topology for the small-shift SSB frequency translator which is essentially a modified form of the conventional image-rejection mixer topology [1, 2] as shown in fig.2. A 90^0 LO phase splitter is used instead of a 0^0 LO splitter, and a 0^0 IF output combiner is used instead of a 90^0 IF hybrid. By considering the phase of the frequency components at various points in the circuit, it can be verified that the modified topology does indeed reject the USB spectral components. The phase at the various points are easily evaluated if we remember that a 90^0 delay in the RF hybrid and LO phase splitter means a phase shift of -90^0 for positive frequency components and $+90^0$ phase shift for the negative components. Many spectral components exist in the circuit, but for clarity only the desired down-converted (LSB) and unwanted up-converted (USB) components at various points in the circuit are shown in fig.3.

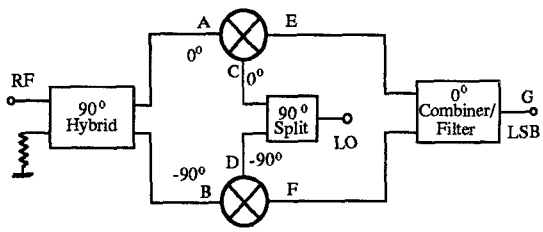


Fig. 1: *The small-shift SSB Frequency Translator*

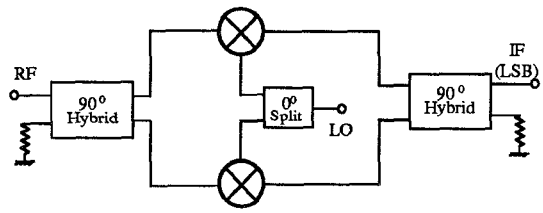


Fig. 2: *The Conventional Image Rejection Mixer*

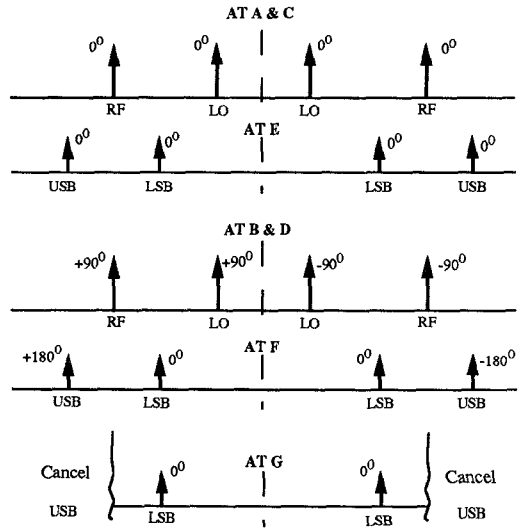


Fig. 3: *Spectra Showing USB Cancellation*

Circuit Design

Two monolithic chips were designed for applications in satellite communications transponders to cover the following frequency bands:

CHIP1	CHIP2
RF: 12.75-14.5GHz	RF: 17.3-18.10GHz
IF: 10.7-12.75GHz	IF: 11.7-12.75GHz
LO: 1.5-3.5GHz	LO: 5.6GHz

A block diagram for the complete design is shown in fig.4. The highly integrated design incorporates RF amplifiers, LO amplifiers, LO phase splitter, balanced FET mixers, 0^0 IF output combiner/filter and the biasing networks all on a single chip.

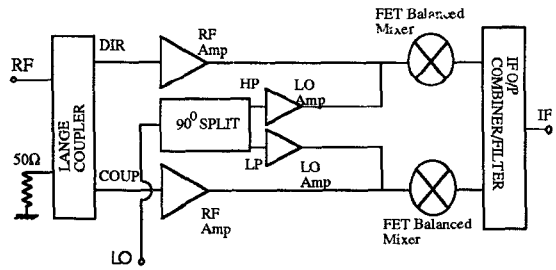


Fig. 4: *Block Diagram of the Complete Design*

The balanced mixer is perhaps the key component in determining the overall chip performance. These usually employ large baluns and considerable attention is therefore being given in the literature for their miniaturisation [3-8]. However, the FET arrangement used here totally eliminates the need for baluns by virtue of its circuit topology. Fig. 5 shows the circuit diagram. This compact arrangement has been shown to offer an FET balanced mixer with a wide-band performance, excellent port VSWR's and isolations in addition to having conversion gain [9, 10].

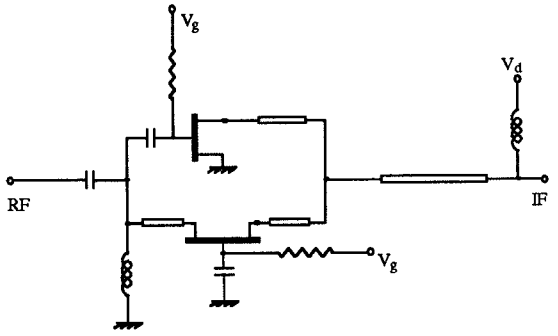


Fig. 5: *CG/CS FET Pair Balanced Mixer*

Another key element is the LO 90^{o} phase splitter which is shown in fig.6. This consists of a lumped element Wilkinson power divider followed by high-pass and low-pass sections to provide the 90^{o} phase difference at the outputs. Feedback amplifiers are also placed at the two outputs which prevent the balanced mixer elements from affecting the LO phase and amplitude balance.

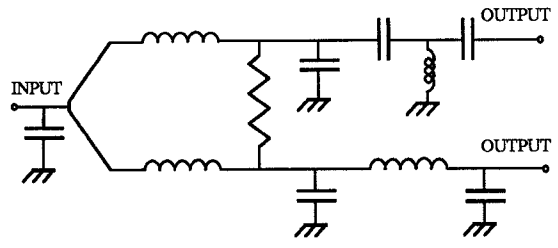


Fig. 6: *90 Degree Phase Splitter*

Fabrication and Measurements

The monolithic chips were fabricated using the GMMT F20 Foundry process. Chip1 which measures 3.7mmx3.2mm, was fabricated on a standard implant GaAs wafer; Chip2 which measures 3mmx3mm, was fabricated on a switch-profile (low gain) GaAs wafer. Photomicrographs of the two chips are shown in fig.7.

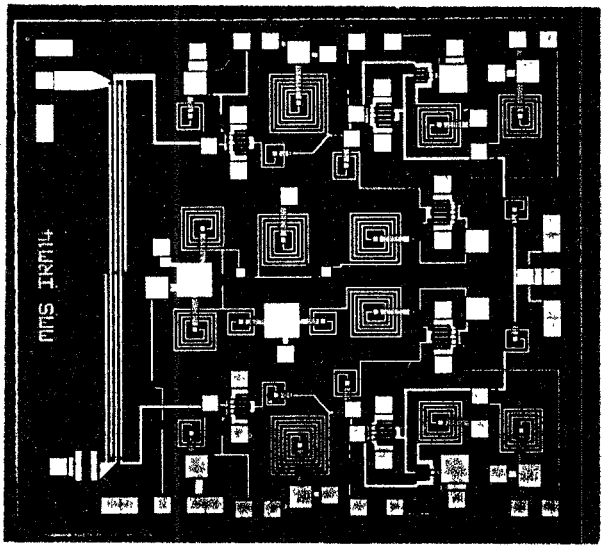
Measurements were made on chip using the Cascade Summit probe station. A maximum LO power of 8dBm was used. Fig.8 shows the relative LSB and USB outputs of the two chips. Chip1 exhibits a LSB conversion gain over the RF range 4.25-13.75GHz, attaining a maximum gain of 5dB at 5GHz (although more gain could have been obtained if more LO power was available). The USB rejection is better than 18dB over a much larger bandwidth.

Chip2 shows a conversion loss of 5+/-2dB over the 16-19.75GHz RF range, and achieves over 23dB of USB rejection. The gain is lower than predicted and this is believed to be because this chip was fabricated on the switch-profile wafer. It was observed during measurements that the FETs had a much higher pinch-off voltage and less gain.

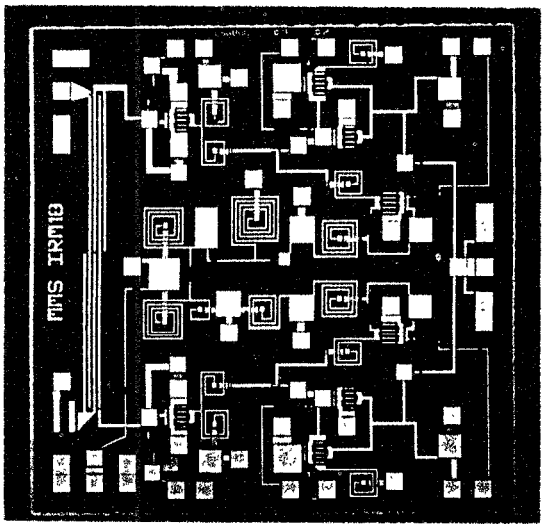
Conclusions

A modified topology for the design of SSB frequency translators requiring IFs higher than the LO have been presented in this paper. Two highly integrated, compact monolithic frequency translator chips have been realised for applications in satellite communications transponders. The associated biasing network and rf/lo amplifiers and IF output combiner/filter are all incorporated on the same chip. The first chip showed

5dB maximum SSB conversion gain with minimum 18dB USB rejection over an RF range of 4.25-13.75GHz. The second chip showed a SSB conversion loss of 5+/-2dB with minimum 23dB USB rejection between 16-19.75GHz. The loss in the second chip is due to the switch-profile (low gain) wafer in which it was fabricated. The wide-band performance of both chips meant that image-rejection was also obtained.



(A) Chip1



(B) Chip2

Fig. 7: *Photomicrographs of the Frequency Translators*

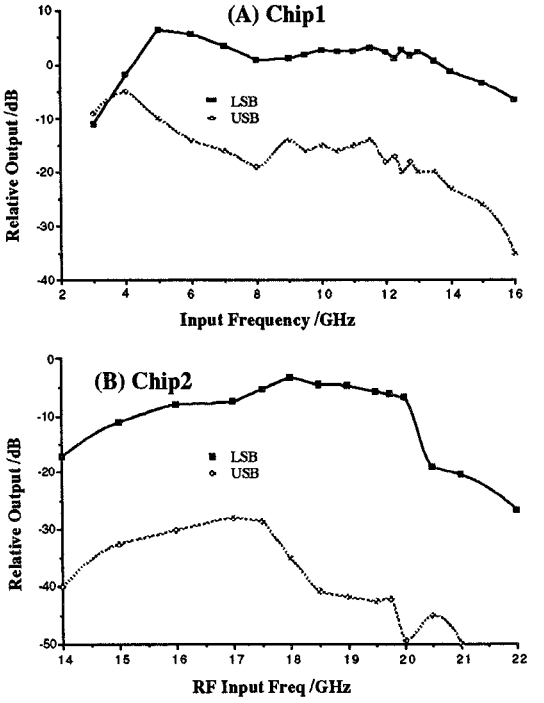


Fig. 8: *Measured LSB & USB Output*

Acknowledgements

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